

What is claimed is:

1. A memory unit, comprising:

first and second access transistors coupled to a bit line pair, wherein the first access transistor comprises a first terminal coupled to one bit line pair, and the second access transistor comprises a first terminal coupled to the other;

a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and

a selection unit having two input terminals coupled to a word line and a flush line, and an output terminal coupled to gates of the first access transistor and the second access transistor, wherein predetermined information is written to the latch node from the bit line pair according to activations of the word line or the flush line.

2. The memory unit as claimed in Claim 1, wherein the selection unit is an OR gate with two terminals coupled to the word line and the flush line respectively and an output terminal coupled to the gates of the first access transistor and the second access transistor.

3. The memory unit as claimed in Claim 1, wherein the latch node comprises a first inverter and a second inverter, the first inverter comprises an input terminal coupled to the second terminal of the second access transistor and an output

5 terminal coupled to the second terminal of the first access
6 transistor, and the second inverter comprises an input
7 terminal coupled to the output terminal of the first inverter
8 and an output coupled to the input terminal of the first
9 inverter.

1 4. The memory unit as claimed in Claim 1, wherein when
2 the flush line is activated during a flush operation, the first
3 access transistor and the second access transistor are turned
4 on, such that the predetermined information is written into
5 the latch from the bit line pair.

1 5. A memory module, comprising:

2 at least one first memory region comprising a plurality
3 of memory units, each memory unit comprising:

4 first and second access transistors coupled to a
5 bit line pair, wherein the first access
6 transistor includes a first terminal coupled
7 to one of the bit line pair, and the second
8 access transistor includes a first terminal
9 coupled to the other;

10 a latch node coupled between second terminals of
11 the first access transistor and the second
12 access transistor to latch data; and

13 a selection unit including a first input terminal
14 coupled to a word line, an output terminal
15 coupled to gates of the first access
16 transistor and the second assess transistor,
17 and a second input terminal;

18 wherein the second input terminals of the selection
19 units in all memory units are coupled to a

20 flush line, and invalidation information is
21 written into the latch nodes in the memory
22 units from the bit line pair when the flush
23 line is activated during a flush operation.

1 6. The memory module as claimed in Claim 5, wherein
2 predetermined information is written to latch node of one of
3 the memory units from the bit line pair when a corresponding
4 word line is activated during a normal operation.

1 7. The memory module as claimed in Claim 5, wherein
2 the selection unit is an OR gate comprising two input terminal
3 coupled to a corresponding word line and the flush line, and
4 an output terminal coupled to the gate of the first access
5 transistor and the second access transistor.

1 8. The memory module as claimed in Claim 5, wherein
2 when the flush line is activated during the flush operation,
3 the first access transistor and the second access transistor
4 are turned on, such that the invalidation information is
5 written to the latch nodes in the first and second memory units
6 from the bit line pair.

1 9. The memory module as claimed in Claim 5, wherein
2 the latch node comprises a first inverter and a second
3 inverter, the first inverter comprises an input terminal
4 coupled to a the second terminal of the second access
5 transistor and an output terminal coupled to the second
6 terminal of the first access transistor, and the second
7 inverter comprises an input terminal coupled to the output
8 terminal of the first inverter and an output coupled to the
9 input terminal of the first inverter.

1 10. The memory module as claimed in Claim 5, further
2 comprising:

3 a D-type Flip-Flop (DFF) receiving and synchronizing a
4 flush signal; and
5 a driving buffer coupled to the DFF to active the flush
6 line according to the flush signal from the DFF.

1 11. A fabricating procedure for a cache memory,
2 comprising:

3 determining conditions for a tag memory in the cache
4 memory according to a desired specification of the
5 cache memory;

6 implementing the tag memory as a memory module according
7 to determined conditions, wherein tag memory
8 comprises a plurality of memory units, each
9 comprising:

10 first and second access transistors coupled to a
11 bit line pair, wherein the first access
12 transistor comprises a first terminal coupled
13 to one bit line pair, and the second access
14 transistor comprises a first terminal coupled
15 to the other;

16 a latch node coupled between second terminals of
17 the first access transistor and the second
18 access transistor to latch data; and

19 an OR gate comprising two input terminals coupled
20 to a word line and a flush line, and an output
21 terminal coupled to gates of the first access
22 transistor and the second assess transistor;
23 wherein invalidation information is written

24 to the all latch nodes in the memory units from
25 the bit line pair according to activation of
26 the flush line;
27 checking whether the implemented tag memory meets the
28 determined conditions; and
29 implementing peripheral elements in the cache memory
30 according to the desired specification of the cache
31 memory;
32 modifying the peripheral elements to match the tag memory
33 such that the peripheral elements meet the desired
34 specification; and
35 simulating integration of the tag memory and the
36 peripheral elements in the cache memory to ensure
37 compliance thereof with the desired specification.

1 12. The fabricating procedure as claimed in Claim 11,
2 wherein the conditions comprise the size and the flush cycle
3 time of the tag memory.

1 13. The fabricating procedure as claimed in Claim 11,
2 wherein the desired specification comprises a number of
3 entries, a desired speed and desired performance for the cache
4 memory.